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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,297	03/01/2002	Barry S. Katz	109176.122	2121

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EXAMINER	
PHAN, THAI Q	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,297	KATZ ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to patent application S/N: 10/087,297, file don 03/01/2001. Claims 1-27 are pending in the action.

Drawings

Drawings filed on 04/29/2002 are acceptable for examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1- 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwasaki et al, US patent no. 5,623,417.

As per claim 1, Iwasaki anticipates a method and system for functional analysis or simulation of a circuit design with feature limitations very identical to the claimed invention. According to Iwasaki, the simulation method includes

Providing a description of a physical design having physical components, signal transfer between them, component identification, and components connectivity (Figs. 2, 3, cols. 4, 9, 10),

Providing a signal transfer description from source to destination (col. 12, line 64 to col. 13, line 67),

Providing a signal transfer description as corresponding to at least a portion of the physical connectivity (col. 13, lines 30-67, for example),

And using the signal or data transfer description to construct computer simulation/analysis of the connected functional components for functional design verification.

As per claim 2, Iwasaki anticipates a logical pin definition including pin names of the identified component (cols. 12-13).

As per claim 3, Iwasaki anticipates part identifications or identified modules in the library for the design and design interface, and verification (cols. 1, 4-5).

As per claims 4-12, Iwasaki anticipates the claimed limitations for the design verification and design interface in the simulation.

As per claim 13, Iwasaki anticipates a method and system for functional analysis or simulation of a circuit design with feature limitations very identical to the claimed invention. According to Iwasaki, the simulation system includes means

Providing a description of a physical design having physical components, signal transfer between them, component identification, and components connectivity (Figs. 2, 3, cols. 4, 9, 10),

Providing a signal transfer description from source to destination (col. 12, line 64 to col. 13, line 67),

Providing a signal transfer description as corresponding to at least a portion of the physical connectivity (col. 13, lines 30-67, for example),

And using the signal or data transfer description to construct computer simulation/analysis of the connected functional components for functional design verification.

As per claim 14, Iwasaki anticipates the physical components including logical pin definition, logical pin names such as inverter, enabling, etc.

As per claims 15-24, Iwasaki anticipates the claimed limitations for design verification and simulation.

As per claims 25 and 26, Iwasaki anticipates a computerized implementation method and system for functional analysis or simulation of a circuit design with feature limitations very identical to the claimed invention. According to Iwasaki, the simulation system includes means and program instructions implemented in the simulator:

Providing a description of a physical design having physical components, signal transfer between them, component identification, and components connectivity (Figs. 2, 3, cols. 4, 9, 10),

Providing a signal transfer description from source to destination (col. 12, line 64 to col. 13, line 67),

Providing a signal transfer description as corresponding to at least a portion of the physical connectivity (col. 13, lines 30-67, for example),

And using the signal or data transfer description to construct computer simulation/analysis of the connected functional components for functional design verification.

As per claim 27, Iwasaki anticipates a method and system for functional analysis or simulation of a circuit design with feature limitations very identical to the claimed invention. According to Iwasaki, the simulation system includes means

Providing a description of a physical design having physical components, signal transfer between them, component identification, and components connectivity (Figs. 2, 3, cols. 4, 9, 10),

Providing a signal transfer description from source to destination (col. 12, line 64 to col. 13, line 67),

Providing a signal transfer description as corresponding to at least a portion of the physical connectivity (col. 13, lines 30-67, for example),

Identifying a physical component corresponding to a source node in the data or signal transfer description (col. 5, lines 43-67, cols. 8-12),

Identifying a set of pins for the identified physical component corresponding to the source node (cols. 6-13),

And using the signal or data transfer description to construct computer simulation/analysis of the connected functional components for functional design verification.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 5,222,030, issued to Dangelo et al, on June 1993
2. US patent no. 5,432,460, issued to Flecha et al, on July 1995
3. US patent no. 5,732,192, issued to Malin et al, on Mar. 1998
4. US patent no. 5,862,149, issued to Carpenter et al, on Jan. 1999
5. US patent no. 6,175,946, issued to Ly et al, on Jan. 2001

6. US patent no. 6,456,628, issued to Greim et al, on Sept. 2002

7. US patent no. 6,510,405, issued to Gilbertson, Roger Lee, on Jan. 2003

8. US patent no. 6,694,464, issued to Quayle et al, on Feb. 2004

9. US patent application publication no. 2002/0112208, issued to Kakizawa et al.

10. US patent application publication no. 2002/0162086, issued to Morgan, David.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 571-272-3783. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 571-272-3780. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sept. 15, 2005

Thai Phan
Patent Examiner